Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 13 (Cancelled)

14. (Previously presented) A digital amplifier, comprising:

a summation circuit for summing an input signal with a feedback signal, and generating a summed output signal;

a noise shaping network with an input coupled to a summation circuit output and generating a noise shaped signal;

a sampling stage with an input connected to a noise shaping network output, and generating a sampled signal, the sampling stage having a predetermined sampling frequency, and generating a sampling stage output signal with a lower transition rate with respect to the sampling frequency by a predetermined multiple;

a feedback loop providing the sampling stage output signal coupled directly to the summation circuit; and

an output stage with inputs connected to a sampling stage output and generating an output signal.

15. (Previously presented) The digital amplifier of claim 14, wherein the output stage includes an H-bridge controller.

16. (Previously presented) The digital amplifier of claim 14, wherein the sampling stage further comprises a logic circuit for suppressing sampling of the input signal for a set number of clock cycles of the sampling frequency clock.

17. (Previously presented) The digital amplifier of claim 16, wherein the logic circuit further includes a transition detector for detecting a transition in the output signal.

18. (Previously presented) The digital amplifier of claim 14, wherein the sampling stage output signal has a multi-state output, with at least three states.

19. (Previously presented) The digital amplifier of claim 14, wherein the noise shaping network comprises a plurality of integrator stages.

20. (Previously presented) A digital amplifier, comprising:

a summation circuit for summing an input signal with a feedback signal, and generating a summed output signal;

a noise shaping network with an input coupled to a summation circuit output and generating a noise shaped signal;

a sampling stage with an input connected to a noise shaping network output, and generating a sampling stage output signal with a multi-state output, with an least three states;

a feedback loop providing the sampling stage output signal of the sampling stage coupled directly to the summation circuit; and

an output stage with inputs connected to a sampling stage output and generating an output signal.

21. (Previously presented) The digital amplifier of claim 20, wherein the output stage includes a semiconductor H-bridge controller.

22. (Previously presented) The digital amplifier of claim 20, wherein the sampling circuit generates a sampling stage output signal with a lower transition rate with respect to the sampling frequency by a predetermined multiple.

23. (Previously presented) The digital amplifier of claim 20, wherein the sampling circuit further comprises a logic circuit for suppressing sampling of the input signal for a set number of clock cycles of the sampling frequency clock.

24. (Previously presented) The digital amplifier of claim 23, wherein the logic circuit further comprises a transition detector for detecting a transition in the output signal.

25. (Previously presented) The digital amplifier of claim 20, wherein the noise shaping network comprises a plurality of integrator stages.

Claims 26 - 28 (Cancelled)

29. (Currently amended) A method of digital amplification, comprising:

summing an input signal with a feedback signal and generating a summed output signal;

noise shaping the summed output signal to generate a noise shaped signal;

sampling the noise shaped signal at a predetermined sampling frequency and generating a sampled output signal with a lower transition rate with respect to the predetermined sampling frequency by a predetermined multiple;

feeding back the sampled output signal as the feedback signal;

outputting the sampled output signal as an output signal; and

~~The method of digital amplification of claim 28, further comprising~~

outputting the sampled output signal through an H-bridge controller.

30. (Currently amended) A method of digital amplification, comprising:

summing an input signal with a feedback signal and generating a summed output signal;

noise shaping the summed output signal to generate a noise shaped signal;

sampling the noise shaped signal at a predetermined sampling frequency and generating a sampled output signal with a lower transition rate with respect to the predetermined sampling frequency by a predetermined multiple;

feeding back the sampled output signal as the feedback signal; and

outputting the sampled output signal as an output signal;

~~The method of digital amplification of claim 28,~~

wherein the sampling includes suppressing sampling of the noise shaped signal for a set number of clock cycles of a sampling frequency clock.

31. (Previously presented) The method of digital amplification of claim 30, wherein the suppressing sampling includes detecting a transition in the sampled output signal.

32. (Currently amended) A method of digital amplification, comprising:

summing an input signal with a feedback signal and generating a summed output signal;

noise shaping the summed output signal to generate a noise shaped signal;

sampling the noise shaped signal at a predetermined sampling frequency and generating a sampled output signal with a lower transition rate with respect to the predetermined sampling frequency by a predetermined multiple;

feeding back the sampled output signal as the feedback signal; and

outputting the sampled output signal as an output signal;

~~The method of digital amplification of claim 28,~~

wherein the outputting includes outputting a multi-state output signal with at least three states.

Claim 33 (Cancelled)

34. (Previously presented) A method of digital amplification, comprising:

summing an input signal with a feedback signal and generating a summed output signal;

noise shaping the summed output signal and generating a noise shaped signal;

sampling the noised shaped signal and generating a sampled output signal;

feeding back the sampled output signal as the feedback signal; and

generating a multi-state output signal having at least three states using the sampled output signal.

35. (Previously presented) The method of digital amplification of claim 34, wherein a semiconductor H-bridge controller generates the multi-state output signal.

36. (Previously presented) The method of digital amplification of claim 35, wherein the sampling includes generating a sampled output signal having a lower transition rate with respect to a sampling frequency by a predetermined multiple.

37. (Previously presented) The method of digital amplification of claim 36, wherein the sampling includes suppressing sampling of the noise shaped signal for a set number of clock cycles of a sampling frequency clock.

38. (Previously presented) The method of digital amplification of claim 37, wherein the suppressing sampling includes detecting a transition in the output signal.

39. (Previously presented) The method of digital amplification of claim 38, wherein the noise shaping includes integrating the summed output signal through a plurality of integrator stages.